IN THE CLAIMS

Please amend and consider the claims as follows:

1. (Currently Amended) A hardware verification method comprising:

obtaining a set of packets to be driven by a device under test;

obtaining a set of timing and relation criteria which determines a sequence in which the packets should be driven by the device under test, wherein obtaining the set of timing and relation criteria is dependent on at least one of when a packet should be transmitted, how long it should take to transmit the packet, and a relation of the packet to other packets;

starting multiple drive loops, each drive loop picking up a packet and forcing the device under test to drive the packet;

starting multiple expect loops, each expect loop determining when to expect a packet driven by the device under test and picking up the expected packet when it arrives;

for each drive loop, confirming that the timing and relation criteria are satisfied prior to allowing the drive loop to force the device under test; and

for each expect loop, checking if the expected packet arrives within a specified time period and raising an error flag if the expected packet does not arrive within the specified time period.

2. (Original) The method of claim 1 wherein allowing the drive loop to force the device under test further includes obtaining permission to drive the device under test.

3. (Original) The method of claim 1 wherein determining when to expect a packet driven by the device under test further includes determining if there is permission to drive the device under test.

4. (Original) The method of claim 1 wherein the device under test is a bus bridge.

5. (Original) The method of claim 1 wherein the device under test is a data switch.

6. (Original) The method of claim 1 further including monitoring an output of the device under test to determine whether a packet driven by the device under test is picked up by one of the expect loops and raising an error flag if the packet is not picked up by one of the expect loops.

7. (Original) The method of claim 1 wherein the expect and drive loops communicate over a bus, the method further comprising monitoring activity on the bus and raising an error flag if the bus is idle for more than a specified time period.

8. (Currently Amended) A hardware verification method comprising:

obtaining a set of packets to be driven by a device under test;

obtaining a set of timing and relation criteria which determines a sequence in which the packets should be driven by the device under test, wherein

obtaining the set of timing and relation criteria is dependent on at least one of when a packet should be transmitted, how long it should take to transmit the packet, and a relation of the packet to other packets;

starting multiple drive loops, each drive loop picking up a packet and forcing the device under test to drive the packet;

starting multiple expect loops, each expect loop determining when to expect a packet driven by the device under test and picking up the expected packet when it arrives;

for each drive loop, confirming that the timing and relation criteria are satisfied prior to allowing the drive loop to force the device under test;

for each expect loop, checking if the expected packet arrives within a specified time period and raising an error flag if the expected packet does not arrive within the specified time period; and

monitoring an output of the device under test to see if a packet driven by the device under test is picked up by one of the expect loops and raising a flag if the packet is not picked up by an expect loop.

9. (Original) The method of claim 8 wherein allowing the drive loop to force the device under test further includes obtaining permission to drive the device under test.

10. (Original) The method of claim 8 wherein determining when to expect a packet driven by the device under test further includes determining if there is permission

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to drive the device under test.

11. (Original) The method of claim 8 wherein the device under test is a bus bridge.

12. (Original) The method of claim 8 wherein the device under test is a data switch.

13. (Original) The method of claim 8 wherein the expect and drive loops communicate over a bus, the method further comprising monitoring activity on the bus and raising an error flag if the bus is idle for more than a specified time period.

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14. (Currently Amended) A hardware verification system, comprising:

at least one drive buffer for holding packets to be driven by a device under test;

at least one expect buffer for holding a set of timing and relation criteria which determines a sequence in which the packets should be driven by the device under test, wherein obtaining the set of timing and relation criteria is dependent on at least one of when a packet should be transmitted, how long it should take to transmit the packet, and a relation of the packet to other packets;

a drive module which starts multiple drive loops that pick up packets from the drive buffer and force the device under test to drive the packets, the drive module ensuring that each drive loop satisfies specified timing and relation criteria prior to allowing the drive loop to force the device under

test; and

an expect module which starts multiple expect loops that pick up packets driven by the device under test, the expect module ensuring that each expect loop satisfies specified timing and relation criteria prior to allowing the expect loop to expect and pick up a packet driven by the device under test, the expect module raising an error flag if the expected packet does not arrive within a specified time period.

15. (Original) The hardware verification system of claim 14 further including a spurious packet checker module which starts a process that checks and raises an error flag if a packet at an output of the device under test is not picked up by an expect loop.

16. (Original) The hardware verification system of claim 14 further including a controller which controls communication between the drive loops, expect loops, and the device under test.

17. (Original) The hardware verification system of claim 14 wherein the device under test is a bus bridge.

18. (Original) The hardware verification system of claim 14 wherein the device under test is a data switch.

19. (Original) The hardware verification system of claim 16 wherein the communication occurs over a bus.

20. (Original) The hardware verification system of claim 19 further comprising a bus idle monitor which monitors activity on the bus and sends an error notification to the controller if the bus is idle for more than a specified time period.